What is claimed is:

1. A method for biasing a body of a transistor, the method comprising:

detecting a voltage applied to a terminal of a transistor; and

coupling a biasing voltage to the body based upon the detected voltage.

2. The method of claim 1, wherein coupling a biasing voltage further comprises, when a gate of the transistor is driven high, applying to the body substantially the voltage applied to the terminal of the transistor.

3. The method of claim 1, wherein coupling a biasing voltage further comprises, when a gate of the transistor is driven low, applying a first voltage lower than the voltage applied to the terminal of the transistor.

4. The method of claim 3, wherein the first voltage is lower than the voltage applied to the terminal of the transistor and but not less than the voltage applied to the terminal of the transistor minus a voltage drop across a parasitic diode in the body of the transistor when the transistor is in an active mode.

5. A circuit, comprising:

a transistor having a first terminal and a body;

a voltage detector that is to detect a terminal voltage that is to be applied to the first terminal of the transistor and that is to apply a bias voltage to the body of the transistor based upon the detected terminal voltage.

6. The circuit of claim 5, wherein the bias voltage is substantially equal to the terminal voltage.

7. The circuit of claim 5, wherein the bias voltage is less than the terminal voltage but not less than the terminal voltage minus a voltage drop across a parasitic diode in the body of the transistor when the transistor is in active mode.

8. A semiconductor circuit, comprising:

a power supply node that is to provide a supply voltage;

at least one field effect transistor having a source, a body, and a gate electrically coupled in a direct current manner to the body; and

the source coupled to the power supply node

9. The circuit of claim 1, wherein the at least one field effect transistor is at least one p-channel field effect transistor (PFET transistor) and the body is an n-type body.

10. The circuit of claim 9, wherein the at least one PFET transistor has a tap coupled to the n-type body and the gate is coupled to the n-type body through the tap.

11. The circuit of claim 9, wherein the tap is n+ type material.

12. The circuit of claim 9, wherein the gate is electrically coupled through a first inverter and a second inverter to the n-type body.

13. The circuit of claim 12, wherein the at least one PFET transistor has a drain, and an electrostatic discharge impulse that is to be received at the drain is to pass through the body of the second inverter.

14. The circuit of claim 9, wherein the at least one PFET transistor is to be forward body biased when the gate is driven low.

15. The circuit of claim 9, wherein the at least one PFET transistor is to be reverse body biased when the gate is driven high.

16. The circuit of claim 9, wherein a threshold voltage of the at least one PFET transistor is to be lowered when the gate is driven by a first voltage.

17. The circuit of claim 9, wherein a threshold voltage of the at least one PFET transistor is to be increased when the gate is driven by a second voltage.

18. A semiconductor circuit, comprising:

a power supply node that is to provide a supply voltage;

a first current source;

at least one field effect transistor having a source, a body coupled to the first current source;

and the source coupled to the power supply node.

19. The circuit of claim 18, wherein the at least one field effect transistor is at least one p-channel field effect transistor (PFET transistor) and the body is an n-type body.

20. The circuit of claim19, wherein the at least one PFET transistor has a gate, and the first current source biases the n-type body when the gate is driven.

21. The circuit of claim 19, wherein the at least one PFET transistor has a gate, and the first current source forward biases the n-type body when the gate is driven low.

22. The circuit of claim 19, wherein the at least one PFET transistor has a gate, and the first current source couples the n-type body to the power supply node when the gate is driven high

23. The circuit of claim 19, wherein the at least one PFET transistor has a gate and a drain, and an electric static discharge received at the drain is isolated from the gate.

24. The circuit of claim 19, wherein the first current source is to lower a threshold voltage of the at least one PFET transistor when the n-type body is driven by a first voltage.

25. The circuit of claim 19, wherein the first current source is to increase a threshold voltage of the at least one PFET transistor when the n-type body is driven by a second voltage.

26. The circuit of claim 19, wherein the at least one PFET transistor has a tap coupled to the n-type body, and the first current source is coupled to the n-type body through the tap.

27. The circuit of claim 26, wherein the tap is n+ type material.

28. The circuit of claim 19, wherein the first current source is a current mirror having a first transistor and a second transistor.

29. The circuit claim 28, wherein the first transistor has a first width that is larger than a second width of the second transistor.

30. A method for biasing a body of a transistor, the method comprising:

selecting one of two voltages to be applied to a terminal of a transistor; and

coupling a biasing voltage to the body based upon the selected voltage.